

	U	1 [1 ]	Document ID	Issue Date	Pages
1	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6396292 B2	20020528	17
2	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6373127 B1	20020416	10
3	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6175241 B1	20010116	17
4	<input type="checkbox"/>	<input checked="" type="checkbox"/>	US 6005777 A	19991221	6

	<b>Title</b>	<b>Current OR</b>	<b>Current XRef</b>
1	Test carrier with decoupling capacitors for testing semiconductor components	324/755	324/754; 324/760; 324/765
2	Integrated capacitor on the back of a chip	257/676	257/666; 257/691; 257/707; 257/719; 257/784; 361/723; 361/734
3	Test carrier with decoupling capacitors for testing semiconductor components	324/755	324/754; 324/760; 324/765
4	Ball grid array capacitor	361/766	174/252; 174/260; 174/261; 257/532; 257/691; 257/698; 257/778; 333/172; 361/760; 361/763; 361/773

	Retrieval Classif	Inventor	S	C	P	2	3	4	5
1		Hembree, David R. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
2		Baudouin, Daniel et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
3		Hembree, David R. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
4		Bloom, Terry R. et al.	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

	Image Doc. Displayed	PT
1	US 6396292	<input type="checkbox"/>
2	US 6373127	<input type="checkbox"/>
3	US 6175241	<input type="checkbox"/>
4	US 6005777	<input type="checkbox"/>

L Number	Hits	Search Text	DB	Time stamp
3	14	passive with devices same chips same encapsula\$3	USPAT; US-PGPUB	2002/08/13 11:06
4	1	passive with devices same chips same encapsula\$3	EPO; JPO; DERWENT; IBM TDB	2002/08/13 11:07
5	89	(capacitors or resistors or inductors) same chips same encapsula\$3	EPO; JPO; DERWENT; IBM TDB	2002/08/13 11:17
6	390	(capacitors or resistors or inductors) same chips same encapsula\$3	USPAT; US-PGPUB	2002/08/13 13:39
7	390	((capacitors or resistors or inductors) same chips same encapsula\$3) not ((capacitors or resistors or inductors) same chips same encapsula\$3)	USPAT; US-PGPUB	2002/08/13 11:17
8	365	((capacitors or resistors or inductors) same chips same encapsula\$3) not ((capacitors or resistors or inductors) same chips same encapsula\$3)) and @ad<=20001230	USPAT; US-PGPUB	2002/08/13 13:40
9	49	(encapsulating with(capacitors or resistors or inductors)) same chips	USPAT; US-PGPUB	2002/08/13 13:47
10	44	((encapsulating with(capacitors or resistors or inductors)) same chips ) and @ad<=20001230	USPAT; US-PGPUB	2002/08/13 13:40
11	20	(encapsulating with(capacitors or resistors or inductors)) same chips	EPO; JPO; DERWENT; IBM TDB	2002/08/13 13:56
12	0	(encapsulating with(capacitors or resistors or inductors)) and (ball adj grid adj array)	EPO; JPO; DERWENT; IBM TDB	2002/08/13 13:57
13	9	(encapsulating with(capacitors or resistors or inductors)) and (ball adj grid adj array)	USPAT; US-PGPUB	2002/08/13 13:57

SENT

L Number	Hits	Search Text	DB	Time stamp
3	14	passive with devices same chips same encapsula\$3	USPAT; US-PGPUB	2002/08/13 11:06
4	1	passive with devices same chips same encapsula\$3	EPO; JPO; DERWENT; IBM_TDB	2002/08/13 11:07
5	89	(capacitors or resistors or inductors) same chips same encapsula\$3	EPO; JPO; DERWENT; IBM_TDB	2002/08/13 11:17
6	390	(capacitors or resistors or inductors) same chips same encapsula\$3	USPAT; US-PGPUB	2002/08/13 13:39
7	390	((capacitors or resistors or inductors) same chips same encapsula\$3) not ((capacitors or resistors or inductors) same chips same encapsula\$3)	USPAT; US-PGPUB	2002/08/13 11:17
8	365	((capacitors or resistors or inductors) same chips same encapsula\$3) not ((capacitors or resistors or inductors) same chips same encapsula\$3)) and @ad<=20001230	USPAT; US-PGPUB	2002/08/13 13:40
9	49	(encapsulating with(capacitors or resistors or inductors)) same chips	USPAT; US-PGPUB	2002/08/13 13:47
10	44	((encapsulating with(capacitors or resistors or inductors)) same chips ) and @ad<=20001230	USPAT; US-PGPUB	2002/08/13 13:40
11	20	(encapsulating with(capacitors or resistors or inductors)) same chips	EPO; JPO; DERWENT; IBM_TDB	2002/08/13 13:56
12	0	(encapsulating with(capacitors or resistors or inductors)) and (ball adj grid adj array)	EPO; JPO; DERWENT; IBM_TDB	2002/08/13 13:57
13	9	(encapsulating with(capacitors or resistors or inductors)) and (ball adj grid adj array)	USPAT; US-PGPUB	2002/08/13 14:18
14	7	(encapsulating with passive) and (ball adj grid adj array)	USPAT; US-PGPUB	2002/08/13 14:24
15	0	(encapsulating with passive) and (ball adj grid adj array)	EPO; JPO; DERWENT; IBM_TDB	2002/08/13 14:24
16	0	(encapsulating with transformers) and (ball adj grid adj array)	EPO; JPO; DERWENT; IBM_TDB	2002/08/13 14:24
17	1	(encapsulating with transformers) and (ball adj grid adj array)	USPAT; US-PGPUB	2002/08/13 14:25
18	1	(encapsulating with coils) and (ball adj grid adj array)	USPAT; US-PGPUB	2002/08/13 14:34
19	289	438/107,108,124,455,614,617.ccls. and bonding and encapsulating and @ad<20001230	USPAT; US-PGPUB	2002/08/13 14:46
20	289	438/107,108,124,455,614,617.ccls. and bonding and encapsulating and @ad<=20001230	USPAT; US-PGPUB	2002/08/13 14:38
21	18	(438/107,108,124,455,614,617.ccls. and bonding and encapsulating and @ad<=20001230) and passive	USPAT; US-PGPUB	2002/08/13 14:46
22	399	257/684,687,690,787.ccls. and bonding and encapsulating and @ad<20001230	USPAT; US-PGPUB	2002/08/13 14:46
23	35	(257/684,687,690,787.ccls. and bonding and encapsulating and @ad<20001230) and passive	USPAT; US-PGPUB	2002/08/13 14:47
24	35	((257/684,687,690,787.ccls. and bonding and encapsulating and @ad<20001230) and passive) not ((438/107,108,124,455,614,617.ccls. and bonding and encapsulating and @ad<=20001230) and passive)	USPAT; US-PGPUB	2002/08/13 14:47

US-PAT-NO: 5355283

DOCUMENT-IDENTIFIER: US 5355283 A

TITLE: Ball grid array with via interconnection

----- KWIC -----

A ball grid array is a type of packaged integrated circuit in which one or more integrated circuit chips (semiconductor dice on which electrically conductive circuitry are formed) are mounted on a surface (top substrate surface) of a substrate, and electrical connection to electrically conductive material not part of the packaged integrated circuit, such as a printed circuit board, is made by an array of solder balls located on a surface of the substrate opposite the surface to which the integrated circuit chip or chips are attached (bottom substrate surface). Passive components such as resistors or capacitors can also be mounted on the top surface of the substrate. The substrate can be a multi-layer substrate, electrically conductive traces and/or regions being formed on a surface of each layer of the substrate, such as described in U.S. Pat. No. 4,975,761 to Chu. The integrated circuit chip or chips and the passive components are typically encapsulated by, for instance, plastic to protect the integrated circuit chip or chips and the passive components from the external environment. The integrated circuit chip or chips are electrically connected to the substrate by wirebonding, tape-automated bonding (TAB), or flip-chip interconnection. Ball grid arrays allow a high density of external chip connections to be made as compared to other

packaged integrated  
circuits having leads extending from the package.

According to the invention, a ball grid array is provided that is less expensive and smaller than previous ball grid arrays. The ball grid array according to the invention includes a substrate on which one or more integrated circuit chips (semiconductor dice on which electrically conductive circuitry is formed) are mounted. Passive components, such as resistors and capacitors, can also be mounted on the substrate. Bond wires connect bond pads on the integrated circuit chip or chips to electrically conductive traces formed on the surface (top surface) of the substrate to which the integrated circuit is mounted. Vias (small concave depressions in insulative material which connect a first conductive region to a second conductive region) are formed in the substrate at locations at which it is desired to make electrical interconnection between traces on the top surface of the substrate and pads formed on the surface (bottom surface) of the substrate opposite the surface on which the integrated circuit chip is mounted. If the substrate is a multilayer substrate, vias can also be formed in the multilayer substrate at locations at which it is desired to make electrical interconnection between electrically conductive traces and/or regions formed on various layers of the multilayer substrate. Electrically conductive material is deposited within the via to electrically connect the traces and/or regions on substrate layers to traces and/or regions on other substrate layers or to pads on the bottom surface of the substrate. The integrated circuit chip or chips and passive components are encapsulated with a resin by, for instance, molding or potting. Solder balls



are formed on the pads on the bottom surface of the substrate. The finished package can be connected to, for instance, a printed circuit board by reflowing the solder balls to form an attachment to electrically conductive material not part of the ball grid array, e.g., traces on the surface of the printed circuit board.

L Number	Hits	Search Text	DB	Time stamp
1	93	package and encapsulating same dispensing	USPAT; US-PGPUB	2002/08/14 10:06
2	2	((("5249354") or ("5355283"))).PN.	USPAT; US-PGPUB	2002/08/14 10:05
3	78	(package and encapsulating same dispensing) and @ad<=20001230	USPAT; US-PGPUB	2002/08/14 10:06

US-PAT-NO: 6022583

DOCUMENT-IDENTIFIER: US 6022583 A

TITLE: Method of encapsulating a wire bonded die

----- KWIC -----

A method of dispensing encapsulant material on a wire bonded die comprises dispensing a series of discrete, single-point droplets and a series of continuous beads within an area bounded by a dam. The encapsulant material spreads out from the droplets and the continuous beads to form an encapsulating layer over the wire bonded die in an area defined by the dam.

In any encapsulant dispensing process, several critical issues must be addressed, including the elimination of any voids or bubbles in the encapsulant material, the dispensing of the correct volume of encapsulant on the part in an accurate and repeatable manner, and the speed of the encapsulation process. Notwithstanding the advances that have been made in liquid encapsulation of wire bonded dies using area array interconnect packages, there is a need for an encapsulation process that substantially eliminates trapped voids or bubbles in the protective encapsulating layer of an advanced wire bonded die which may lead to premature part failure. There is also a need for an encapsulation process that relatively quickly and evenly dispenses liquid encapsulant in a predefined pattern to provide an overall level encapsulation of advanced wire bonded dies. Additionally, there is also a need for an encapsulation process

that provides substantially uniform and repeatable encapsulation of wire bonded dies for high volume integrated circuit packaging applications. Moreover, there is a need for an encapsulation process that permits increased flowrates of encapsulating material to be used which results in a higher volume of parts through the encapsulation process.

To these ends, in accordance with a preferred method of the present invention, a combination including a wire bonded die mounted on a carrier substrate is encapsulated with liquid encapsulant. The combination of the wire bonded die and carrier substrate includes a trough extending about an outer periphery of the die, and a dam extending about an outer periphery of the trough. Liquid encapsulant material is dispensed in a predetermined pattern within an area bounded by the dam to form an encapsulating layer over the wire bonded die.

The dispensing pattern preferably includes a series of discrete, single-point dispensing locations which at least partially overlies a top surface of the die and a series of continuous dispensing lines which at least partially overlies an area defined between the trough and the dam. The liquid encapsulant spreads out from each of the single-point dispensing locations and continuous dispensing lines to fully encapsulate the wire bonded die.

With the preferred dispensing pattern of the present invention, an encapsulation process is provided that substantially eliminates trapped voids or bubbles in the protective encapsulating layer over the wire bonded die which may cause early failure of the part. The encapsulation method of the present invention dispenses liquid encapsulant relatively quickly and evenly with increased flowrates to provide an overall level

encapsulated part. The method of the present invention further provides substantially uniform and repeatable encapsulation of wire bonded dies for high volume integrated circuit packaging applications.

Referring to FIG. 1, a preferred method of encapsulating wire bonded die 26 with viscous encapsulant material 16 is shown in accordance with the principles of the present invention. Preferably, the encapsulation process is automated by a programmable and calibrated encapsulant dispensing system (not shown) which dispenses the encapsulant material 16 in a defined pattern and in controlled weight amounts through a dispensing needle 46. A preferred encapsulant dispensing system for use in the present invention is the MILLENIUM.TM. Series Encapsulation Dispensing System commercially available from Asymtek of Carlsbad, Calif. Briefly, the MILLENIUM.TM. Series Dispensing System is a precision dispensing system which provides a closed-loop control of key process parameters for in-line integrated circuit package encapsulation. The positioning and movement of dispensing needle 46 in x-y-z planes is fully programmable, and the weight of encapsulant material 16 that is dispensed at each dispensing location is precisely controlled. The operation and programming functions and syntax of the MILLENIUM.TM. Series Encapsulant Dispensing System are fully described in the MILLENIUM.TM. Series Operating Manuals and the MILLENIUM.TM. Series FLUID MOVE FOR WINDOWS.TM. Programming Manuals which are commercially available from Asymtek and incorporated herein by reference in their entirety. While the MILLENIUM.TM. Series Encapsulant Dispensing System is a preferred encapsulant dispensing system for use in the

present invention, it is contemplated that other automated encapsulant

dispensing systems may be used without departing from the spirit and scope of the present invention.

Still referring to FIG. 1, a preferred dispensing pattern for encapsulating wire bonded die 12 in accordance with the present invention is shown. The

dispensing needle 46 is programmed to dispense five weight-controlled droplets of encapsulant material 16, shown diagrammatically at 48a-48e, in a predefined sequence that corresponds respectively to five discrete, single point

dispensing locations 50a-50e. In particular, dispensing needle 46 is preferably operable to move under programmed control of the automated

dispensing system to each of the discrete, single-point dispensing locations

50a-50e, starting at dispensing location 50a and moving successively to each of the dispensing locations 50b-50d before ending at dispensing location 50e.